Intersil

THE IH5009 SERIES OF LOW COST ANALOG SWITCHES

INTRODUCTION

The IH5009 series of analog switches described in this note were designed by Intersil to fill the need for an easy-to-use, inexpensive switch for both industrial and military applications. Although low cost was one of the primary design objectives (less than $1/switch in volume), performance and versatility have not been sacrificed. Up to four channels per package are available, no external power supplies are required, and switching speeds are guaranteed to be less than 500 ns.

CIRCUIT OPERATION

Switching Virtual Ground Signals

The signals seen at the drain of a junction FET type analog switch can be arbitrarily divided into two categories: Those which are less than ±200 mV, and those which are greater than ±200 mV. The former category includes all those circuits where switching is performed at the virtual ground point of an op-amp, and it is primarily towards these applications that the IH5009 family of circuits is directed. In applications where the signal amplitude at the switch is greater than ±200 mV, the simple design of the IH5009 is no longer appropriate and a more complex switch design is called for. See REF. 1 for a complete discussion of this type of switch.

It is important to realize that the ±200 mV limitation applies *only* to the signal at the drain of the FET switch; signals of ±10V or greater can be commutated by the IH5009 in a circuit of the type shown in Figure 1. For a high gain inverting amplifier the signal level at the virtual ground point will only be a few microvolts for ±10V input and output swings.

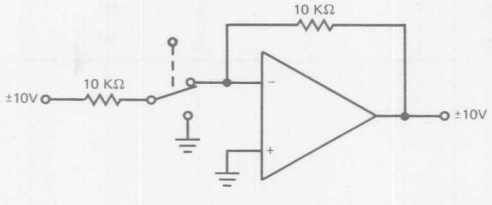

FIGURE 1. SWITCHING AT VIRTUAL GROUND POINT

The Compensating FET

Those devices which feature common drains (IH5009, 5010, 5013, 5014, etc.) have another FET in addition to the channel switches (Figure 2). This FET, which has gate and source connected such that $V_{GS} = 0$, is intended to compensate for the on-resistance of the switch. When placed in series with the feedback resistor (Figure 3) the gain is given by

$$\text{GAIN} = \frac{10\ \text{k}\Omega + R_{DS}\ (\text{compensator})}{10\ \text{k}\Omega + R_{DS}\ (\text{switch})}$$

Clearly, the gain error caused by the switch is dependent on the match between the FETs rather than the absolute value of the FET on-resistance. For the standard product,

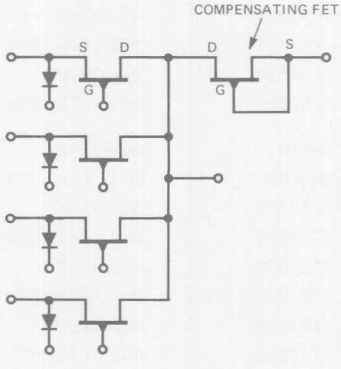

FIGURE 2. SCHEMATIC OF IH5009 & IH5010

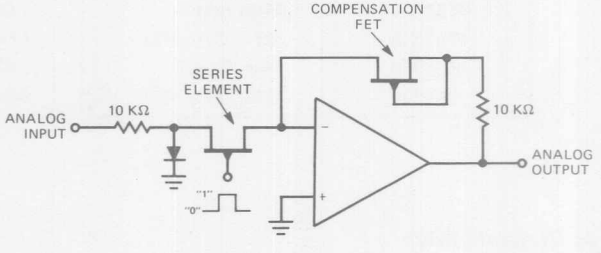

FIGURE 3. USE OF COMPENSATION FET

all the FETs in a given package are guaranteed to match within 50Ω. Selections down to 5Ω are available however. The part numbers are shown in Table I. Since the absolute value of $R_{DS\,(ON)}$ is only guaranteed to be less than 100Ω or 150Ω, it is clear that a substantial improvement in gain accuracy can be obtained by using the compensating FET. This is only true however when the input resistor and the feedback resistor are similar in value: for dissimilar values, the benefits of the compensating FET are less pronounced.

INTERSIL INC., 10900 N. TANTAU AVE., CUPERTINO, CA. 95014 (408) 257-5450 TWX 910-338-0028

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TABLE I

PART NUMBER	INPUT LOGIC DRIVE	DESCRIPTION	EFFECTIVE $r_{DS(ON)}$ (OHMS) MAX.	$r_{DS(ON)}$ (OHMS) MAX.
IH5009	High Level	4-Channel, 15V Logic	50	100
IH5010	DTL, TTL, RTL	4-Channel, 5V Logic	50	150
ITS7318	High Level	4-Channel, 15V Logic	25	100
ITS7319	DTL, TTL, RTL	4-Channel, 5V Logic	25	150
ITS7320	High Level	4-Channel, 15V Logic	10	100
ITS7321	DTL, TTL, RTL	4-Channel, 5V Logic	10	150
ITS7322	High Level	4-Channel, 15V Logic	5	100
ITS7323	DTL, TTL, RTL	4-Channel, 5V Logic	5	150
IH5013	High Level	3-Channel, 15V Logic	50	100
IH5014	DTL, TTL, RTL	3-Channel, 5V Logic	50	150
ITS7324	High Level	3-Channel, 15V Logic	25	100
ITS7325	DTL, TTL, RTL	3-Channel, 5V Logic	25	150
ITS7326	High Level	3-Channel, 15V Logic	10	100
ITS7327	DTL, TTL, RTL	3-Channel, 5V Logic	10	150
ITS7328	High Level	3-Channel, 15V Logic	5	100
ITS7329	DTL, TTL, RTL	3-Channel, 5V Logic	5	150
IH5017	High Level	2-Channel, 15V Logic	50	100
IH5018	DTL, TTL, RTL	2-Channel, 5V Logic	50	150
ITS7330	High Level	2-Channel, 15V Logic	25	100
ITS7331	DTL, TTL, RTL	2-Channel, 5V Logic	25	150
ITS7332	High Level	2-Channel, 15V Logic	10	100
ITS7333	DTL, TTL, RTL	2-Channel, 5V Logic	10	150
ITS7334	High Level	2-Channel, 15V Logic	5	100
ITS7335	DTL, TTL, RTL	2-Channel, 5V Logic	5	150
IH5021	High Level	1-Channel, 15V Logic	50	100
IH5022	DTL, TTL, RTL	1-Channel, 5V Logic	50	150
ITS7336	High Level	1-Channel, 15V Logic	25	100
ITS7337	DTL, TTL, RTL	1-Channel, 5V Logic	25	150
ITS7338	High Level	1-Channel, 15V Logic	10	100
ITS7339	DTL, TTL, RTL	1-Channel, 5V Logic	10	150
ITS7340	High Level	1-Channel, 15V Logic	5	100
ITS7341	DTL, TTL, RTL	1-Channel, 5V Logic	5	150

Logic Compatibility

The 5009 through 5024 series parts are primarily intended for constant – impedance multiplexing. The diode connected to the J-FET source acts like a shunt switch, while the FET itself acts as a series switch. The advantage of this configuration is its high noise immunity when the series element is off. The diode then clamps the source to +0.7V with a low AC impedance to ground and prevents false triggering of the FET for positive inputs. Negative inputs present no problems since they further increase the OFF voltage beyond pinch-off.

The even-numbered devices in the family (5010 through 5024) are designed for interfacing with 5V logic. The pinch-off of the FETs is selected to be less than 3.9V (V_P @ I_D = 1 nA); therefore, a positive logic level +4.5V will supply adequate safety margin for proper gating action. To guarantee this +4.5V from series 54/74 TTL logic requires the use of a pull-up resistor: Values from 2 kΩ to 10 kΩ are suitable depending upon the speed requirements (Figure 4). Alternatively the TTL may be operated from +6V supplies. The "1" level will then be greater than +4.5V without the

need for a pull-up resistor. The maximum on-resistance is guaranteed for +0.5V on the gate of the FET. Since the maximum low level output voltage from TTL is 0.4V, the ON-resistances specified are conservative. With 0V applied to the FET gate, typical ON-resistances of 90Ω will be obtained.

The odd-numbered devices in the family (5009 through 5023) are designed for interfacing with 15V logic. The pinch-off of these parts is selected to be less than 10V, so that a +11V positive logic level provides adequate safety margin. To obtain this level from open collector TTL logic also requires a pull-up resistor; 1 kΩ to 10 kΩ is suitable depending on the speed and fan-out requirements (Figure 5). The ON-resistance is measured with +1.5V applied to the gate and is guaranteed to be less than 100Ω at 25°C. For 0V on the gate, the typical R_{ON} is 60Ω.

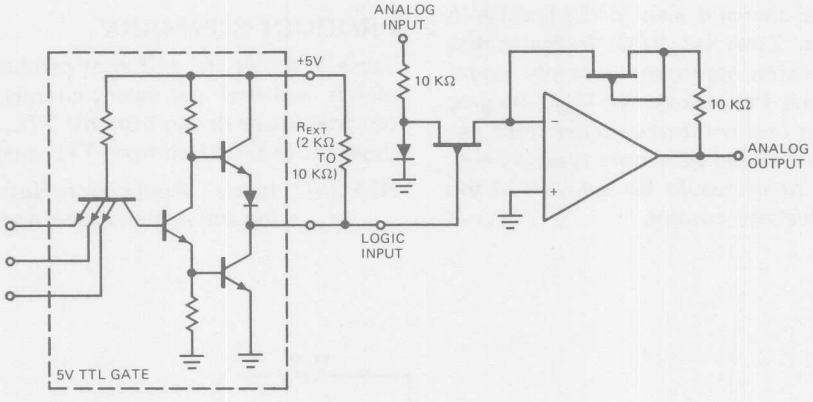


FIGURE 4. INTERFACING WITH +5V LOGIC

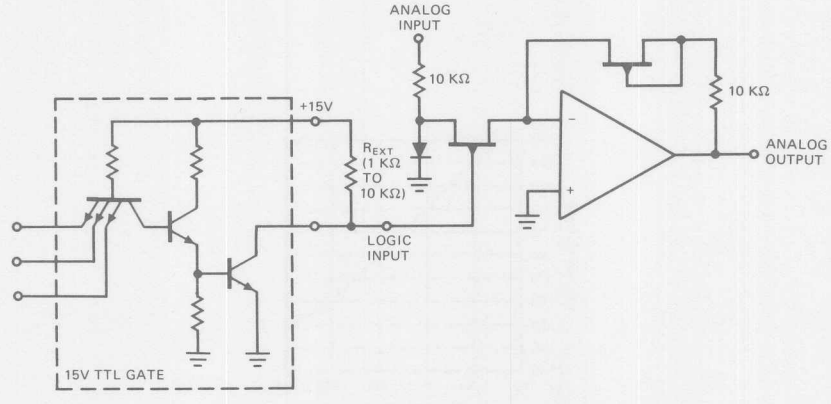


FIGURE 5. INTERFACING WITH +15V OPEN COLLECTOR LOGIC

In applications where low ON-resistance is critical, special selections can be made. Since high pinch-off FETs have lower ON-resistances than low pinch-off types (for a given geometry) it is advantageous to make such selections from the odd-numbered devices and use high level TTL for the control logic.

Maximum Switch Current

The maximum current through the switch is dictated primarily by leakage considerations rather than power dissipation problems. When the drain of the FET is held at virtual ground, current through the channel tends to bias the source positive. Eventually, the source-gate junction will forward bias, giving rise to large leakage currents. This is most likely to occur at high temperature when the junction turn-on potential is at its lowest. The data sheet guarantees maximum leakage for I_S = 1 mA and 2 mA, with V_{IN} = 0V. The substantial increase seen in the leakage in changing I_S from 1 mA to 2 mA (at 70°C) indicates that the turn-on potential is being approached rapidly under these conditions. Specifying the leakage for V_{IN} (the gate potential) = 0V is a worst case condition; under most circumstances V_{IN} = +200 mV would be a more typical value. Thus 200 mV additional signal would be required at the source to give the same leakage current.

Switching Speed and Crosstalk

The switching speed is guaranteed to be less than 500 ns at 25°C. Typical turn-on and turn-off times are 150 ns and 300 ns, respectively.

When analog switches are used in conjunction with operational amplifiers, settling time is often an important parameter. In a typical fast amplifier, settling times of 1 μs to 0.1% are seen. This time is primarily caused by non-linear modes of operation within the amplifier, and the inclusion of an analog switch at the virtual ground point will not cause significant degradation of the settling time.

Crosstalk can be measured using the circuit of Figure 6. At low frequencies, it is very difficult to obtain accurate values since the separation is better than 120 dB. Typical crosstalk as a function of frequency is shown in Figure 7.

PRODUCT SUMMARY

Table 2 shows the different product numbers, their schematics, and their equivalent circuits. The even numbers are designed to be driven from 5V TTL, while odd numbers are designed to be driven from TTL open collector logic (15V).

REF [1]: Intersil Application Note A003: *"Understanding and Applying the Analog Switch".*

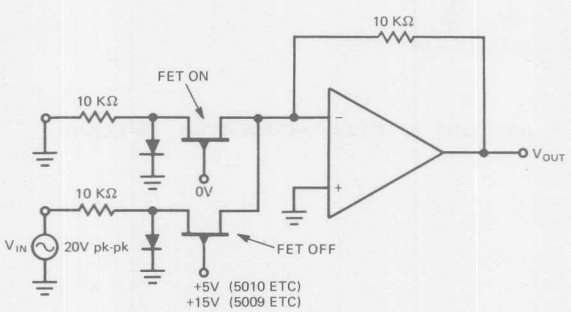


FIGURE 6. CROSSTALK MEASUREMENT CIRCUIT

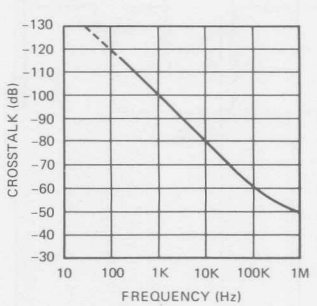
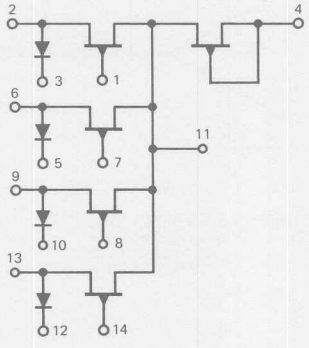


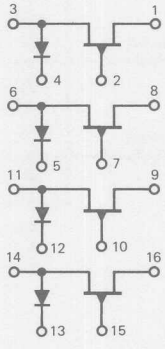
FIGURE 7. CROSSTALK AS A FUNCTION OF FREQUENCY

TABLE II

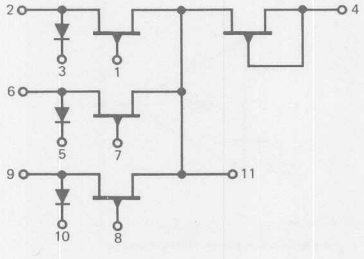
IH5009 ($r_{DS(ON)} \leq 100\Omega$)
IH5010 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN SILICONE DIP



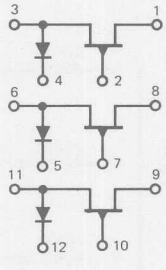
IH5011 ($r_{DS(ON)} \leq 100\Omega$)
IH5012 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN SILICONE DIP



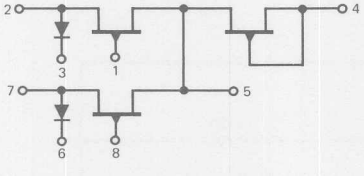
IH5013 ($r_{DS(ON)} \leq 100\Omega$)
IH5014 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN SILICONE DIP



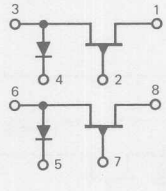
IH5015 ($r_{DS(ON)} \leq 100\Omega$)
IH5016 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN SILICONE DIP



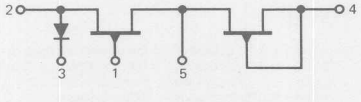
IH5017 ($r_{DS(ON)} \leq 100\Omega$)
IH5018 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN SILICONE DIP



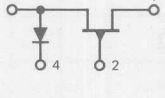
IH5019 ($r_{DS(ON)} \leq 100\Omega$)
IH5020 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN SILICONE DIP

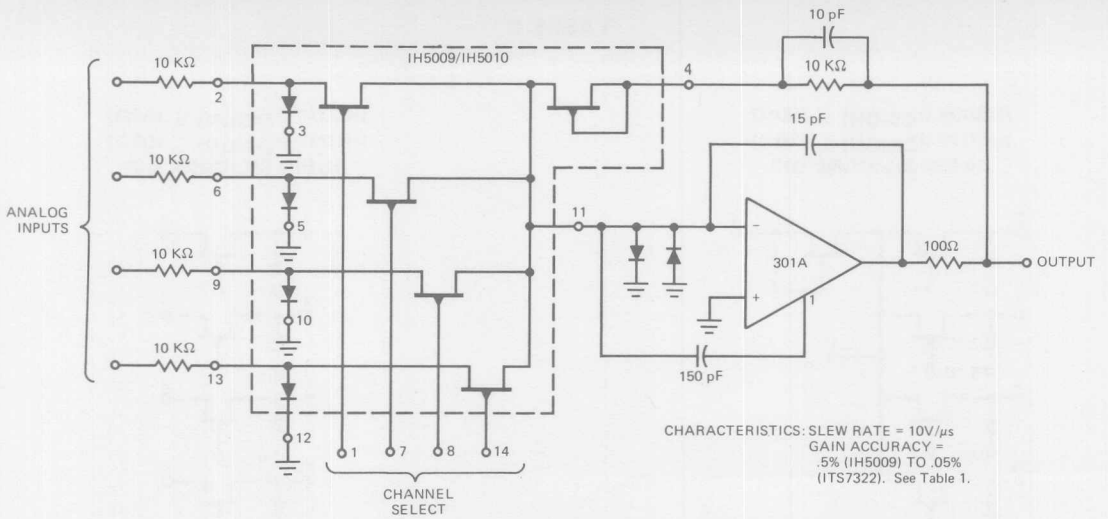


IH5021 ($r_{DS(ON)} \leq 100\Omega$)
IH5022 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN SILICONE DIP

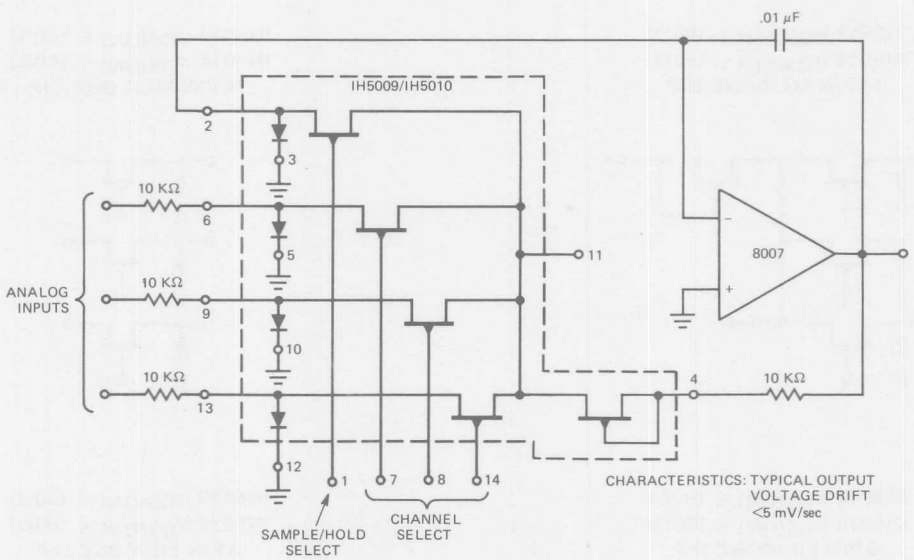


IH5023 ($r_{DS(ON)} \leq 100\Omega$)
IH5024 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN SILICONE DIP

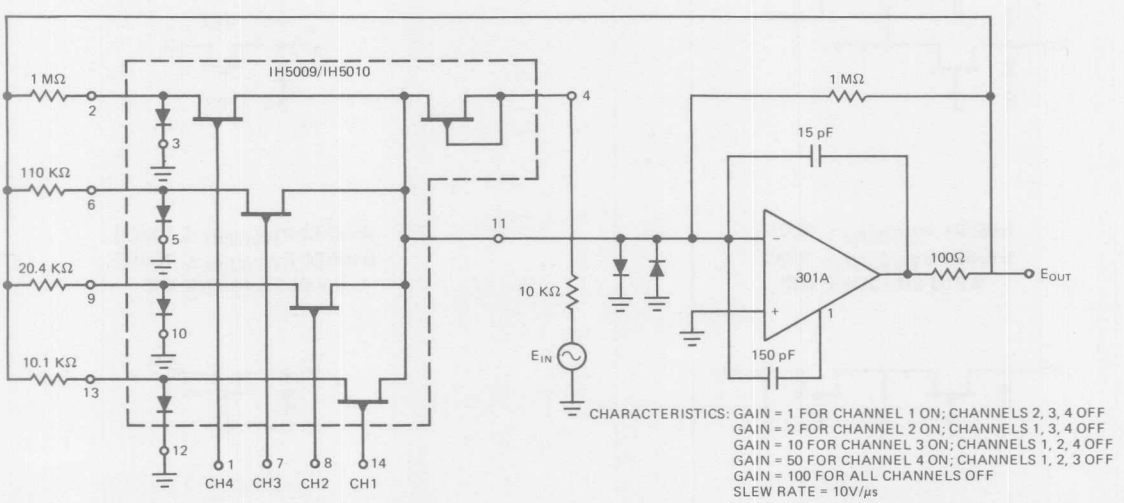




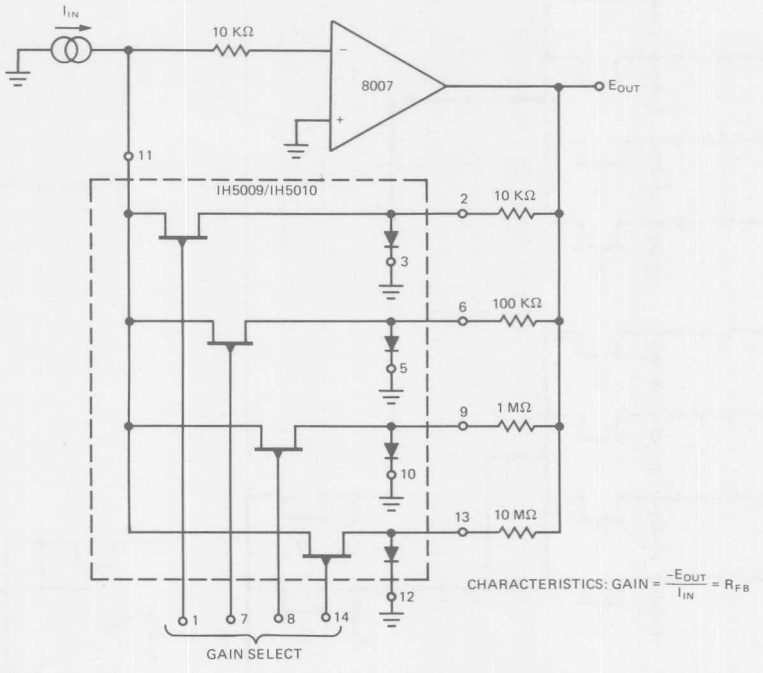
LOW COST 4 CHANNEL MULTIPLEXER



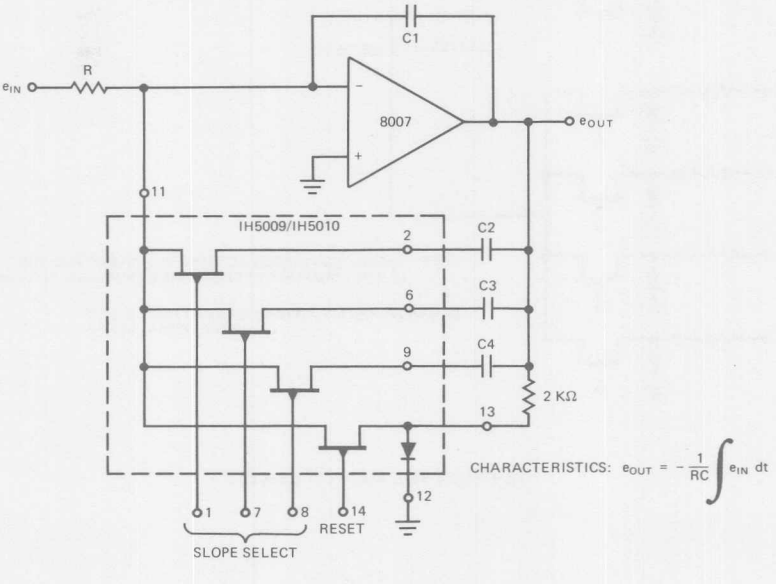
3 CHANNEL MULTIPLEXER WITH SAMPLE & HOLD



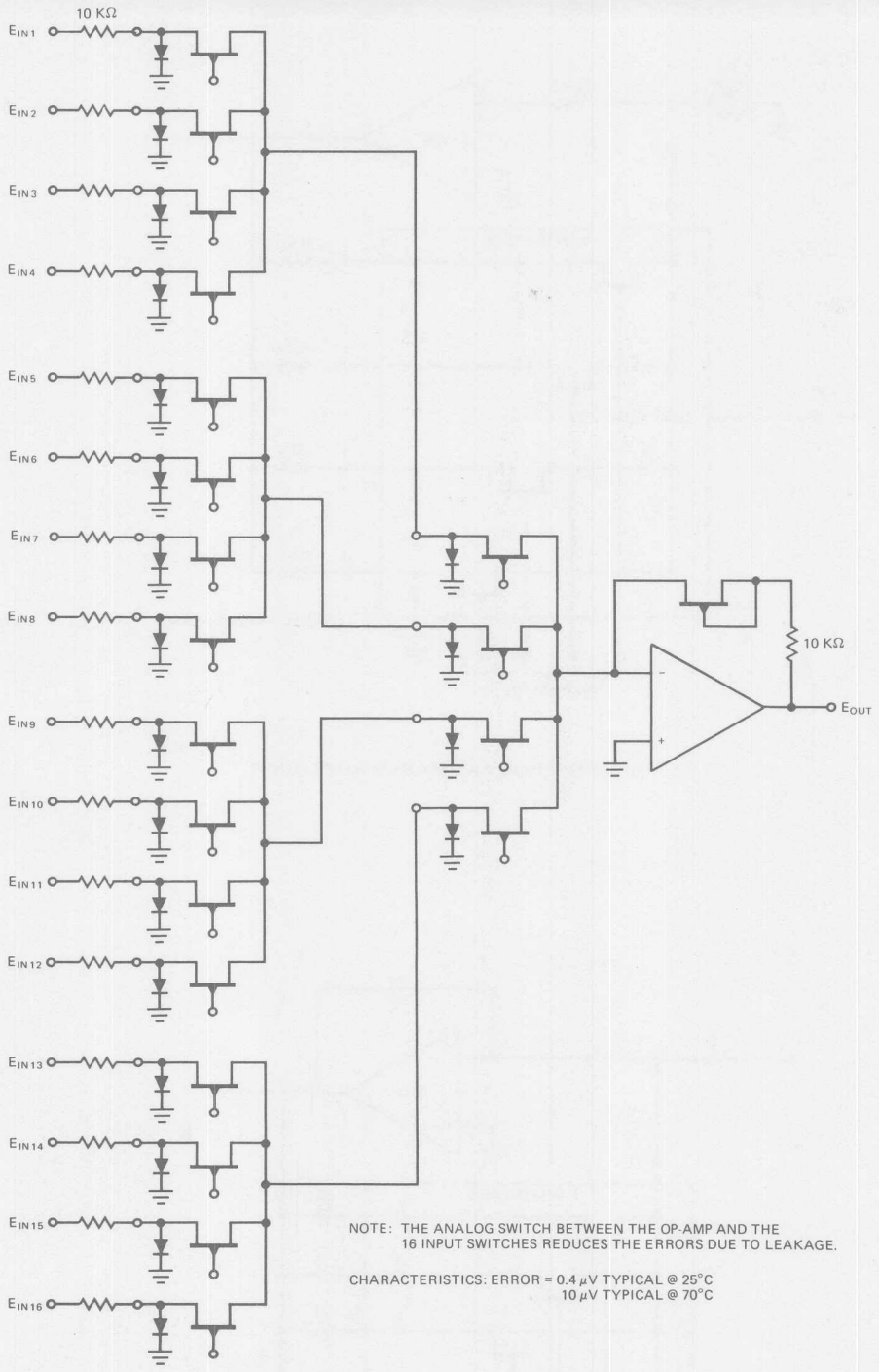
GAIN RANGING CIRCUIT



GAIN PROGRAMMABLE AMPLIFIER



PROGRAMMABLE INTEGRATOR WITH RESET



NOTE: THE ANALOG SWITCH BETWEEN THE OP-AMP AND THE 16 INPUT SWITCHES REDUCES THE ERRORS DUE TO LEAKAGE.

CHARACTERISTICS: ERROR = 0.4 μV TYPICAL @ 25°C
10 μV TYPICAL @ 70°C

16 CHANNEL MULTIPLEXER